The HMP8154EVAL1 Encoder Evaluation Platform

Application Note | July 1997 | AN9743

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Features

- HMP8154 Video Encoder
- Digital Parallel ITU-R BT.656 Input
- 50 Pin, Dual Row Receptacle
- Analog Output Formats
  - Y/C + Two Composite
  - RGB + Composite (SCART)
- NTSC and PAL Operation
- ITU-R BT.601 and Square Pixel Operation

Description

The HMP8154EVAL1 encoder evaluation platform is a small (index card size) printed circuit board designed to demonstrate the capabilities and performance of the HMP8156 and HMP8154 and HMP8170-73 NTSC/PAL encoders. The board includes an encoder, voltage references and decoupling, analog output filters, and I/O connectors.

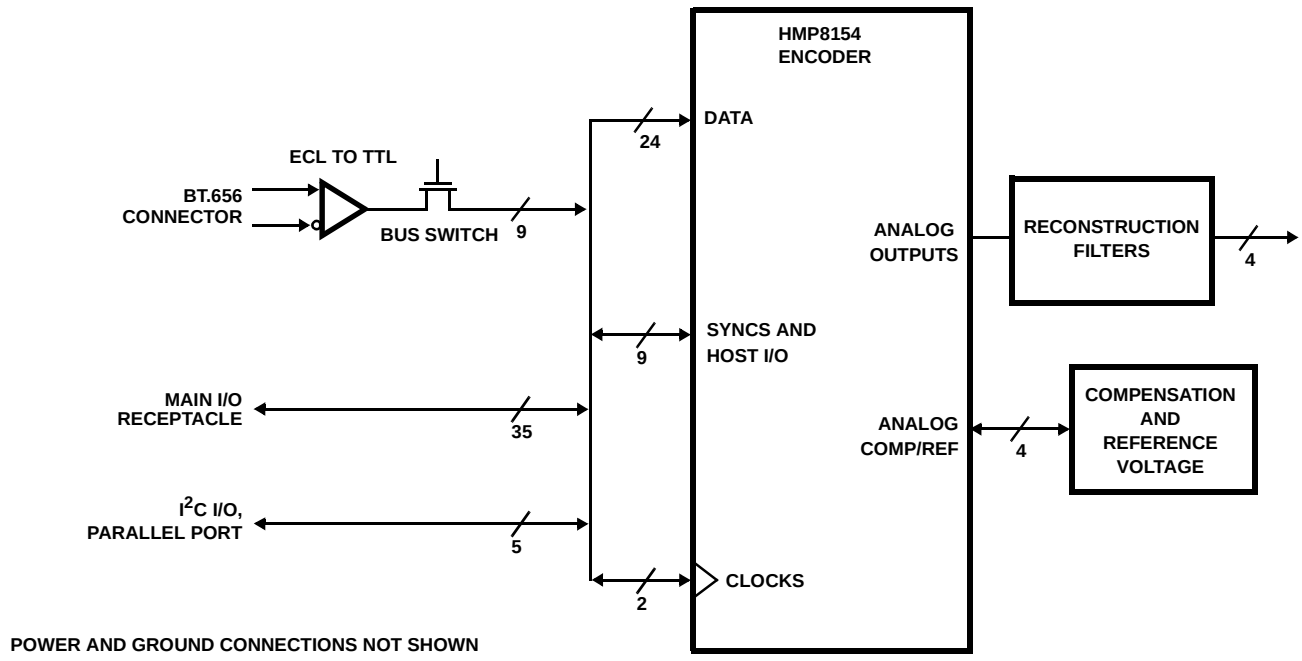
The board's primary input is via a 50 pin receptacle. It may be used for wiring the board into an existing system. The connector provides access to all of the encoder's digital I/O signals.

The board outputs analog video via four coax connectors. The board can output one composite video signal and either S-Video and a second composite signal, or component RGB video.

The board also accepts a digital parallel BT.656 data stream. Translators convert the ECL input to TTL levels and drive the encoder. The encoder converts the data and its embedded timing information into analog video.

For non-default operation, the encoder must be programmed via the I^2C bus. Application software to drive the I^2C bus via the parallel port of a PC is provided with the evaluation kit.

Board Block Diagram



Operating Modes

The HMP8154EVAL1 board has two main operating modes. It may be installed on a mother board as a daughter card or it may be connected with other system components as a stand-alone board.

Stand-Alone BT.656 Operation

In stand-alone mode, the HMP8154EVAL1 is connected to external power supplies, a BT.656 signal generator, a PC parallel port, and a monitor or measurement equipment. The interconnections are shown in Figure 1.

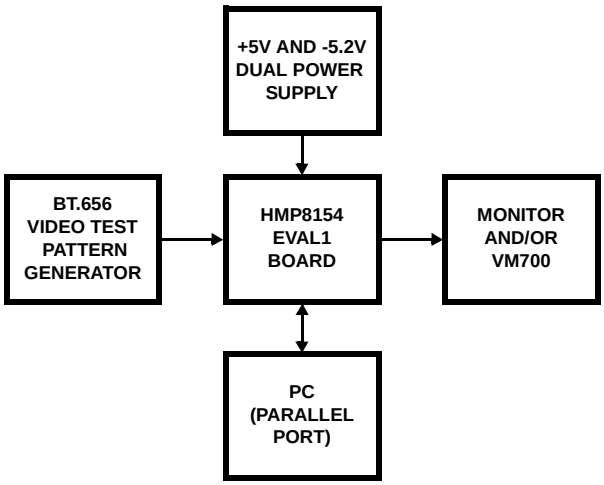


FIGURE 1. STAND-ALONE INTERCONNECTIONS

The test pattern generator may be any that generates digital parallel YCbCr video per the ITU-R BT.656 (formerly CCIR-656) standard. The BT.656 interface uses differential signals with ECL logic levels. It includes 8 or 10 bits of data and a 27.0MHz clock.

For best results, use a linear power supply with isolated dual outputs. The power required is 5.0V ±5% at 300mA and -5.2V ±10% at 150mA. The board grounds are tied together so the power supplies' should not be. The power supply connections are shown in Figure 2. The connections should be made with 20-24 AWG twisted pair wires.

In stand-alone BT.656 mode, the encoder must be programmed for non-default operation. The board includes a header which provides access to the encoder's host interface bus. The header is designed to interface with a standard PC parallel port. The PC is then used to program the encoder via its I^2C interface. Application software included with the evaluation kit is used to program the encoder. It is described in the *Application Software* section below.

Any high quality monitor may be used to observe the encoder's performance. The encoder supports NTSC and PAL displays that have composite, S-Video, or component RGB inputs. An oscilloscope and video measurement equipment are also useful. In all cases, the board's outputs should be terminated with a 75Ω load.

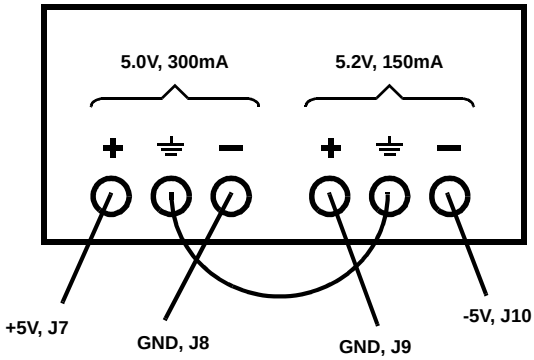


FIGURE 2. POWER SUPPLY CONNECTIONS

Daughter Card Operation

The HMP8154EVAL1 board has a 50 pin, two row receptacle which allows connection into an existing system. The main connector provides access to all of the encoder's digital inputs and outputs. The daughter card uses its own output connectors as in stand-alone mode.

When installed on a mother board, the daughter card's BT.656 interface must be disabled. The bus switch may be opened by installing a jumper shunt on the board at location JP6. The switch may also be opened by asserting its disable signal on the main connector - P1, pin 14.

The HMP8156EVAL2 is the Intersil designed mother board for the HMP8154EVAL1. The mother board is a standard size PC add in card with an ISA bus interface and application software. The HMP8156EVAL2 kit is a complete system which allows demonstrating all of the encoder's operating modes. It has analog video inputs for composite, S-video, and component RGB signals. The analog signals are converted/decoded to the digital domain and input to the daughter card. The board also provides a 3 megabyte video RAM for image capture and display and a BT.656 connector and interface.

Application Software

In stand-alone BT.656 mode, the encoder must be programmed for non-default operation. The board includes a header which provides access to the encoder's host interface bus. The header is designed to interface with a standard PC parallel port. Application software is provided to control the I^2C bus via the parallel port.

The board must be connected to the PC printer port and a clock source in order for the application software to operate correctly. The pixel clock may be driven from the main connector (P1), the BT.656 connector (J1), or the clock connector, (J2). Without an active clock, the encoder will not respond to I2C commands.

The evaluation kit includes two software applications to program the encoder and observe its internal registers. One is a DOS program with a simple command line interface which will run on any PC. The other is a windows program which will only run on PCs using Win95™.

TABLE 1. EXAMPLE DCIIC COMMANDS

FUNCTION	DCIIC USAGE	EXAMPLE DOS COMMAND AND OUTPUT
Reset	dciic -r	c:\hmp8154> dciic -r c:\hmp8154>
Load Configuration	dciic *filename*	c:\hmp8154> dciic bt656.cfg dciic: bt656.cfg loaded. c:\hmp8154>
Read I^2C Register	dciic -i *sub-address*	c:\hmp8154> dciic -i 0 dciic: read: 0x40,0X00 = 0x54 c:\hmp8154>
Write I^2C Register	dciic -i *sub-address value*	c:\hmp8154> dciic -i 2 0x1c dciic: wrote: 0x40,0X02 = 0x1c c:\hmp8154>
Help	dciic -?	c:\hmp8154> dciic -? usage: dciic [options] [file.cfg ...] reads or writes i2c registers. options: [-r] do chip reset [-p <port_adrs>] set printer port base address [-s <slv_adrs>] set device slave address [-i <regAdrs> [<data>]] c:\hmp8154>

DCIIC DOS Application Program

DCIIC (Daughter card I^2C) is a simple DOS program written in C. The program allows the user to:

1. Assert the encoder's $\overline{\text{RESET}}$ signal to initialize the part to its default operating state,
2. Load the encoder's programmable registers from a configuration file, and
3. Read and/or write any of the encoder's programmable registers individually.

By default, the program writes to the parallel port located at PC I/O space address 0x378. If the board is connected to a port which is not located at the default address, then the -p option must be included with the other command line arguments. Other common locations for the parallel port are addresses 0x3bc and 0x278.

When dciic starts, it searches for an encoder by reading the product ID register at register sub-address 0 for slave addresses 0x40 and 0x42. If the encoder does not respond, the program prints an error message and exits. The slave address may be set from the command line using the -s option. If set from the command line, the program does not read the product ID register.

The dciic configuration files are ASCII files which may be edited with any text editor. They have the same format as those used by the HMP8156EVAL2 MMVideoEval software application. However, dciic only supports a subset of the commands -- namely the SetReg command. Any other commands are silently ignored.

The dciic SetReg command consists of the case-sensitive keywords "SetReg CHMP8154" followed by the register sub-address and its value. The numeric values follow the usual C conventions for decimal, octal, or hexadecimal bases. An example command is below:

SetReg CHMP8154 4 0x28

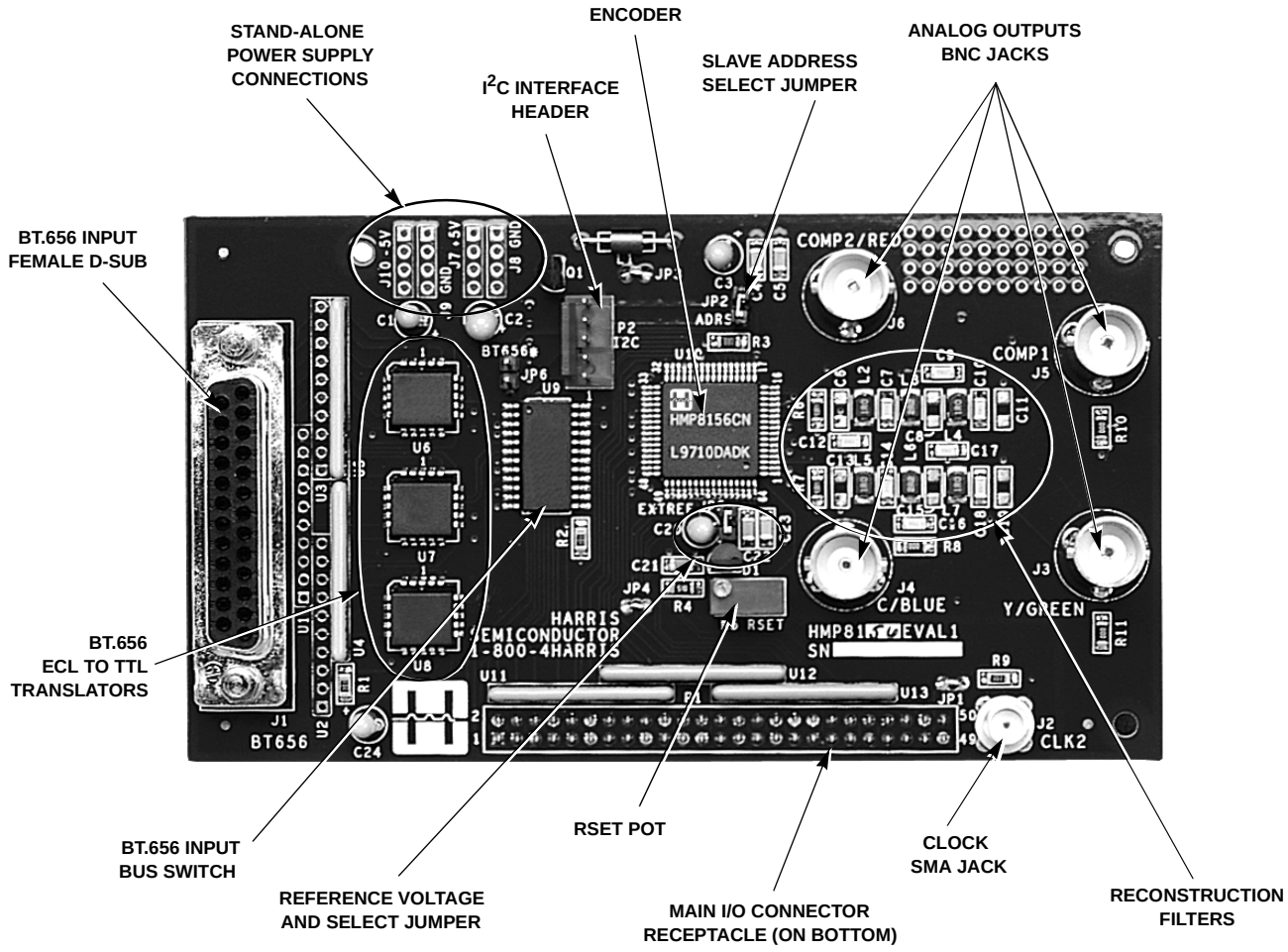
If a different encoder is used on the board, then its part number should be substituted in the second keyword, *i.e.* "CHMP8156" instead of "CHMP8154"

Although written in standard ANSI C, the dciic program was written for compilation using Microsoft Visual C++, version 1.52. The source code is included with the evaluation kit.

MMEncEval Win95 Application Program

The MMEncEval application program for Win95 is not complete at this time. When complete, its interface will be very similar to the MMVideoEval application program used with the HMP8156EVAL2 frame grabber evaluation platform.

Physical Interfaces



Interface Connectors

The HMP8154EVAL1 board's interface connectors are listed in Table 2. In the table, the column titled "Board Part Number" lists a manufacturer and part number of the connector component installed on the board. On some boards, equivalent components may be substituted. The "Mating Part Number" column lists a typical connector which will interconnect correctly with the component installed on the board.

The P1 and P2 connectors do not have standard pin numbers. The pin numbers and locations are shown in Figure 3. The signals for each pin are listed in Tables 3 and 4.

TABLE 2. INTERFACE CONNECTOR DEFINITION

INTERFACE NAME	CONNECTOR STYLE	BOARD PART NUMBER	MATING PART NUMBER	COMMENTS
Main, P1	50 pin, Dual Row	Receptacle AMP 2-635585-1	Header AMP 2-102973-5	Industry standard receptacle and header using 0.025 inch square posts with 100 mil pin spacing.
I^2C, P2	5 pin, Single Row	Header, Molex 22-23-2051	Receptacle housing, Molex 22-01-3057; and Contacts, Molex 08-55-0102	Header and receptacle are keyed and include the locking ramp. Some Molex documentation defines pin 1s on opposite ends of the header and housing.
BT656, J1	25 pin, D-Subminiature	Sockets, AMP 745967-7	Pins, AMP 747912-2	Connectors and pinout defined by ITU-R BT.656 standard.
CLK, J2	SMA Coaxial	Jack, Johnson Components 142-0701-211	Plug, Johnson Components 142-0403-011	The clock interface is bidirectional. The connector must not be driven when the BT656 interface is active or when the Main connector clock pin is driven.
Analog Outputs, J3-J6	BNC Coaxial	Jack, Amphenol 31-5329	Plug, Amphenol 68175	Terminate each analog output with a 75Ω load from the center conductor to the cable shield for best results.
Power, J7-J10		Plated thru-holes in PCB	Stranded Wire, 20 - 24 AWG	When not powered via the main P1 connector, the board may be wired to external power supplies.

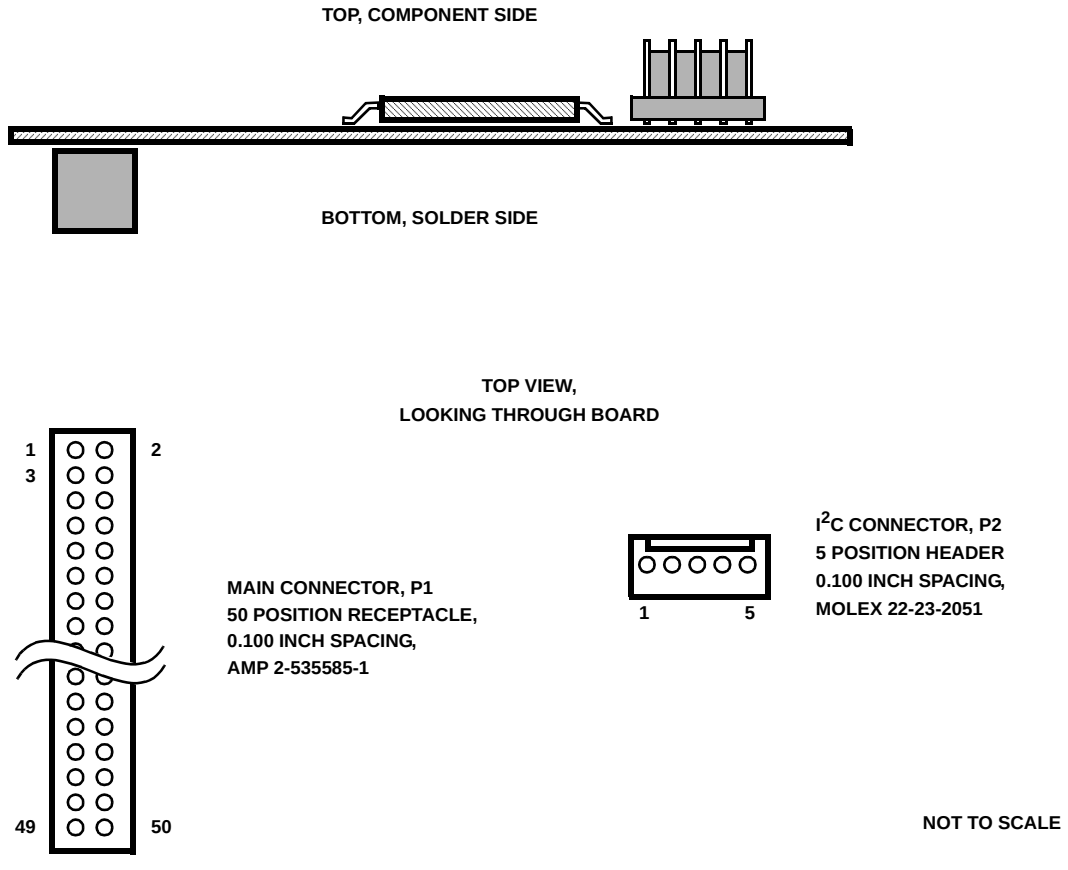


FIGURE 3. MAIN AND I^2C CONNECTOR PIN LOCATIONS.

TABLE 3. MAIN CONNECTOR P1 PINOUT

SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN
V_{CC}	1	PIX<12>	18	PIX<1>	35
GND	2	PIX<11>	19	PIX<0>	36
N/C	3	PIX<10>	20	V_{CC}	37
V_{EE}	4	PIX<9>	21	GND	38
PIX<23>	5	PIX<8>	22	N/C	39
PIX<22>	6	-VSYNC_ENC	23	-BLANK_ENC	40
PIX<21>	7	GND	24	FIELD_ENC	41
PIX<20>	8	V_{CC}	25	N/C	42
PIX<19>	9	V_{CC}	26	SCLK	43
PIX<18>	10	GND	27	SDATA	44
PIX<17>	11	-HSYNC_ENC	28	N/C	45
PIX<16>	12	PIX<7>	29	-RESET_A	46
GND	13	PIX<6>	30	PIXCLK	47
-BT656_ENA (V_{CC})	14	PIX<5>	31	VIDCLK	48
PIX<15>	15	PIX<4>	32	GND	49
PIX<14>	16	PIX<3>	33	V_{CC}	50
PIX<13>	17	PIX<2>	34		

TABLE 4. I^2C CONNECTOR P2 PINOUT

NAME	(NOTE 1) BOARD HEADER PIN NUMBER	(NOTE 1) RECEPTACLE HOUSING PIN NUMBER	(NOTE 2) PC PARALLEL PORT PIN NUMBER	COMMENTS
Reset	1	5	4	The reset signal is active low. It should be asserted for at least four CLK cycles following board powerup.
Output Enable	2	4	3	The serial data signal (and the encoder's SDATA I/O pin) is driven low when the output enable signal is asserted. Otherwise, it is pulled high by an on board resistor.
Ground	3	3	18	Signal return path.
Serial Data	4	2	12	For the encoder, serial data is bidirectional; for the PC, it is only an input.
Serial Clock	5	1	2	The encoder SCLK signal. The encoder pixel clock signal must also toggle for the I^2C interface to operate.

NOTES:

1. Different versions of the Molex documentation for the board header shows pin 1 on either end of the connector. The documentation for the receptacle housing shows pin 1 on the end opposite of the one chosen for the header. Therefore, the pins are reversed so that when connected, pin 1 of the header aligns with pin 5 of the housing.
2. The standard PC parallel port uses a 25 pin D-subminiature connector with sockets. A cable end connector which will interconnect with the PC is part 747912-2 from AMP.

Moveable Jumpers

The board uses several movable jumpers to control its operation and connectivity. The jumpers and the functions they control are described in Table 5.

TABLE 5. JUMPER FUNCTIONS

NAME	FUNCTION		NOTES
	OPEN	SHUNTED	
JP1 Clock	-	J2 is connected to CLK2	3
JP2 I2C Slave Address	Encoder responds to slave address 0x40.	Encoder responds to slave address 0x42.	4
JP3, JP4 Ground	-	Digital and analog grounds connected.	3
JP5 External Reference	Encoder uses its internal reference voltage.	Encoder reference voltage is driven by the board's reference circuit.	4, 5
JP6 BT.656	BT.656 clock and data drivers may be enabled.	BT.656 clock and data drivers are disabled.	6, 7

NOTES:

3. Jumper is hardwired and should not be changed.
4. Default position is shunted.
5. The relation between the reference voltage and output current is described in the encoder's data sheet.
6. Default position is open.
7. The BT.656 driver enable signal is also connected to the main P1 connector pin 14 and to a resistor to ground.

Adjustable Components

The board uses a single potentiometer, R5, to set the RSET value and thus the encoder's full scale output current. The resistor should be adjusted so that the output voltage measured at the load is $1.0V_{PP}$ from the sync tip to the white level. The resistor is set at the factory for correct video levels when driving the board reconstruction filter and an external 75Ω terminator.

The adjustable resistor is not needed when the filter and load are fixed. The adjustment is provided on the board only to allow flexibility to support different, changeable, loads. As shown in the encoder's data sheet, the variability of the output levels is small. They remain within video tolerances when using a fixed 1% tolerance resistor.

Schematics and Layout

The board schematics are shown in Figures 4-10. Notes in the schematics indicate assembly options. The parts list follows in the HMP8154EVAL1 Evaluation Board Parts List.

The board consists of four layers laid out to optimize the performance of the encoder. The top and bottom layers are signal trace layers. The inner layers are used for power and ground planes. The art work for the board is shown in Figures 11-15.

The power plane is split into three sections for V_{EE}, V_{CC}, and V_{AA}. V_{CC} and V_{EE} are powered by the main connector or by external supplies. V_{AA} is connected to V_{CC} via a single ferrite bead. Each section of power plane includes its own bulk area capacitors to ground for decoupling.

The ground plane is split into two sections for digital and analog grounds. Although isolated in their own planes, the two ground areas are **not** electrically distinct. The ground planes are connected via a solid wire at one point.

Intersil customers may use any part of the schematics or layout. Electronic versions are also available.

HMP8154EVAL1 Evaluation Board Schematic Diagrams

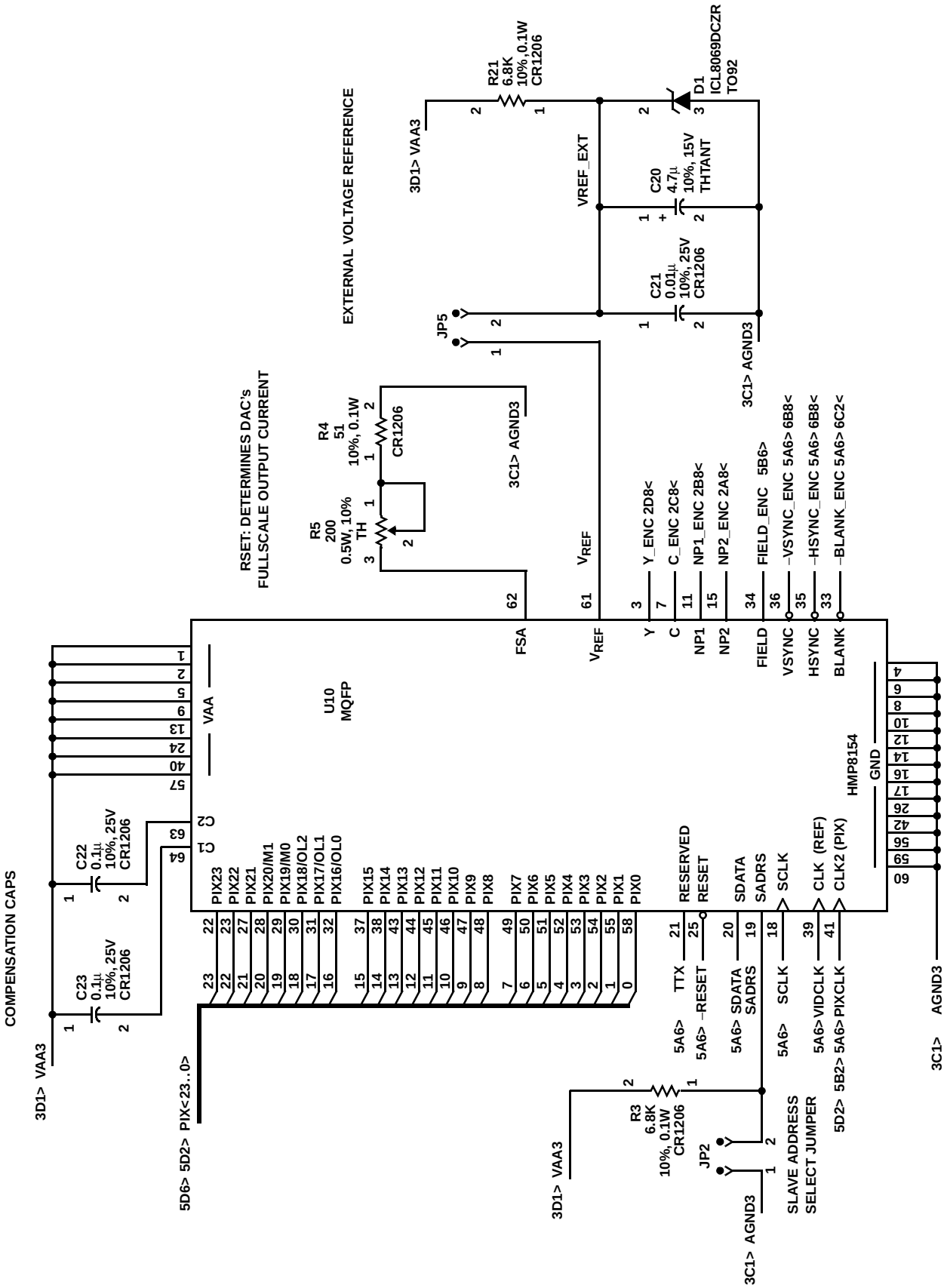
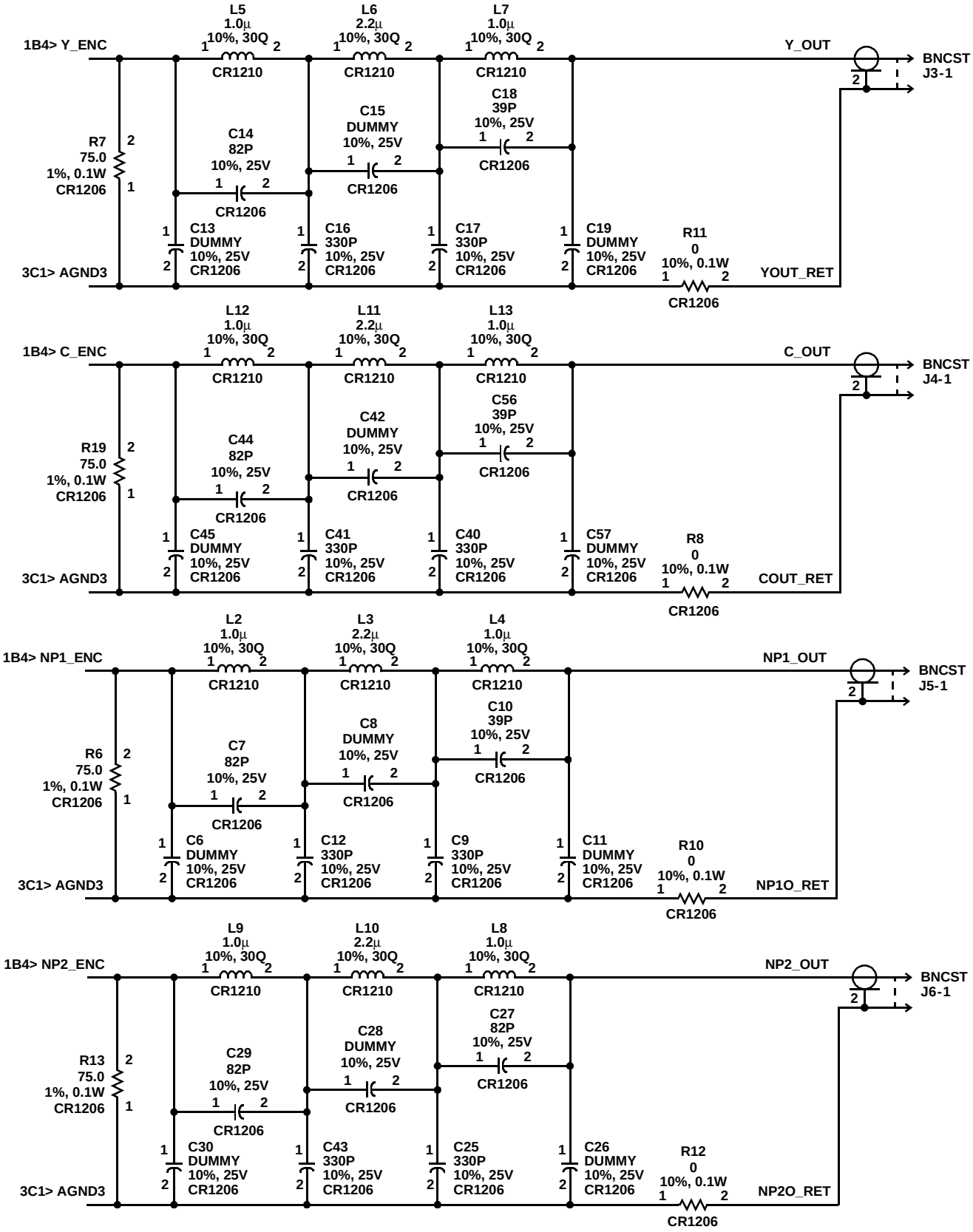


FIGURE 4. ENCODER

HMP8154EVAL1 Evaluation Board Schematic Diagrams (Continued)



NOTE: Caps valued "dummy" are not populated. Components may be added/changed to test alternate reconstruction filter circuits.

FIGURE 5. ANALOG OUTPUTS

HMP8154EVAL1 Evaluation Board Schematic Diagrams (Continued)

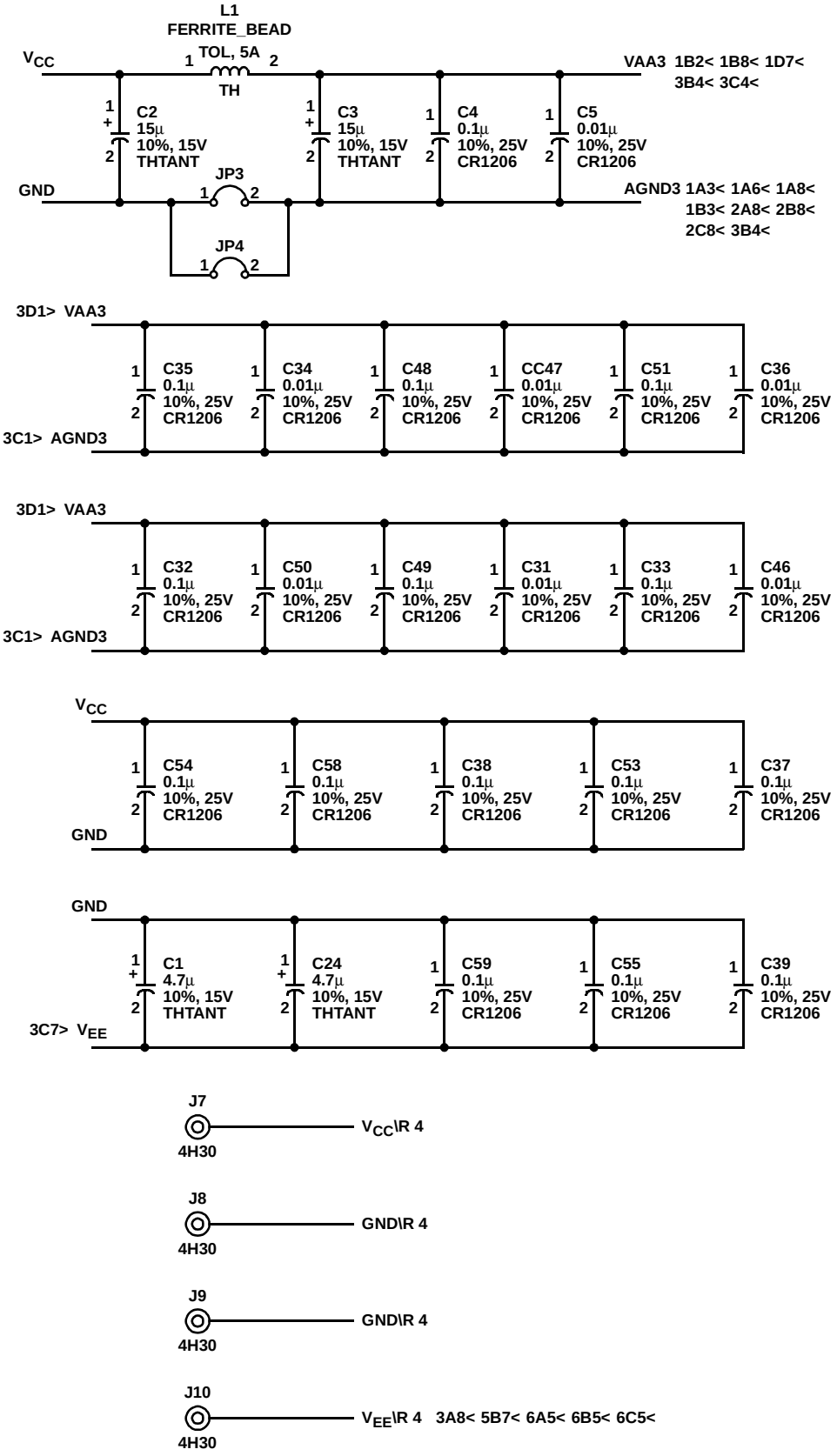


FIGURE 6. POWER/GND

HMP8154EVAL1 Evaluation Board Schematic Diagrams (Continued)

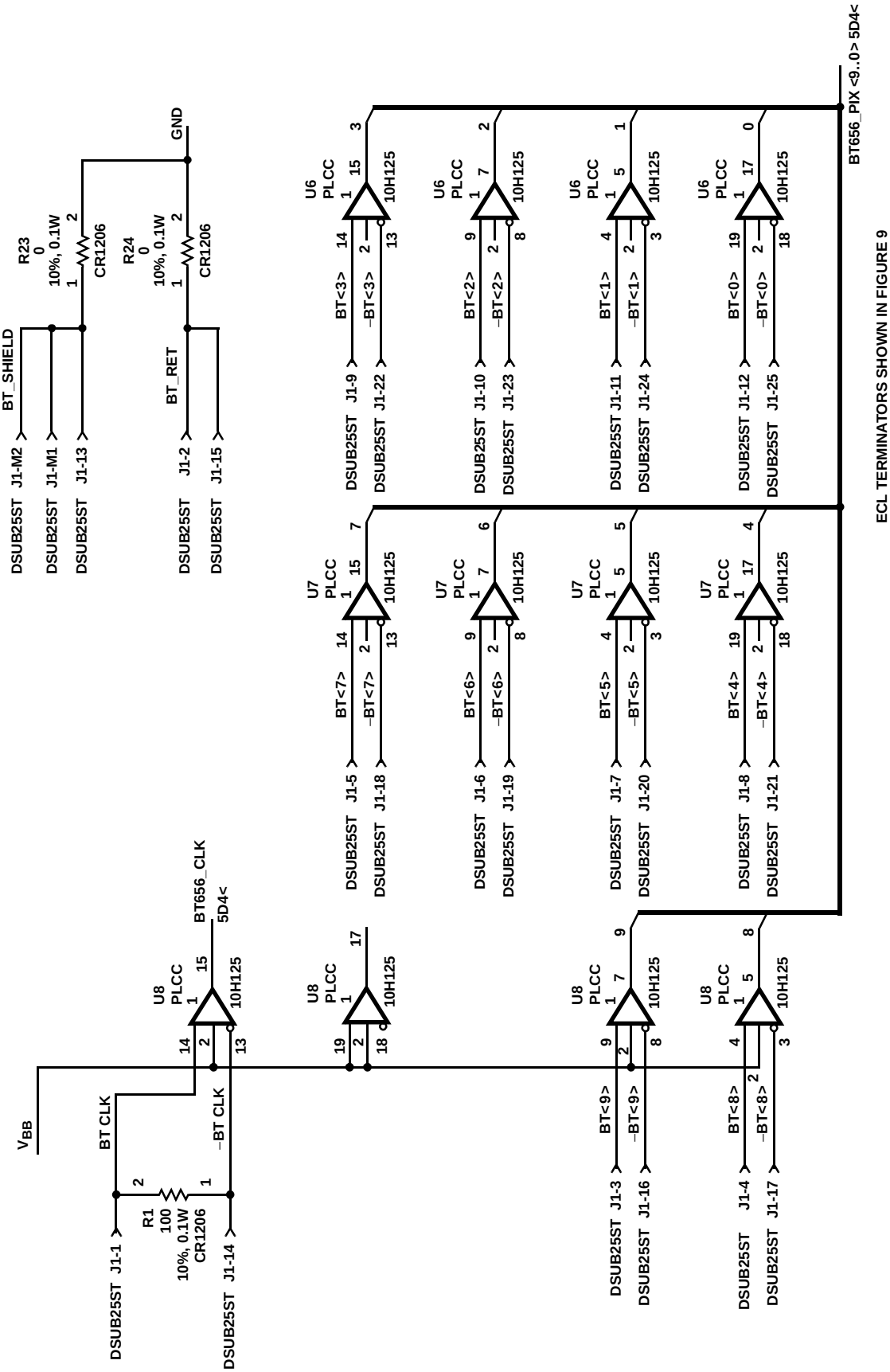
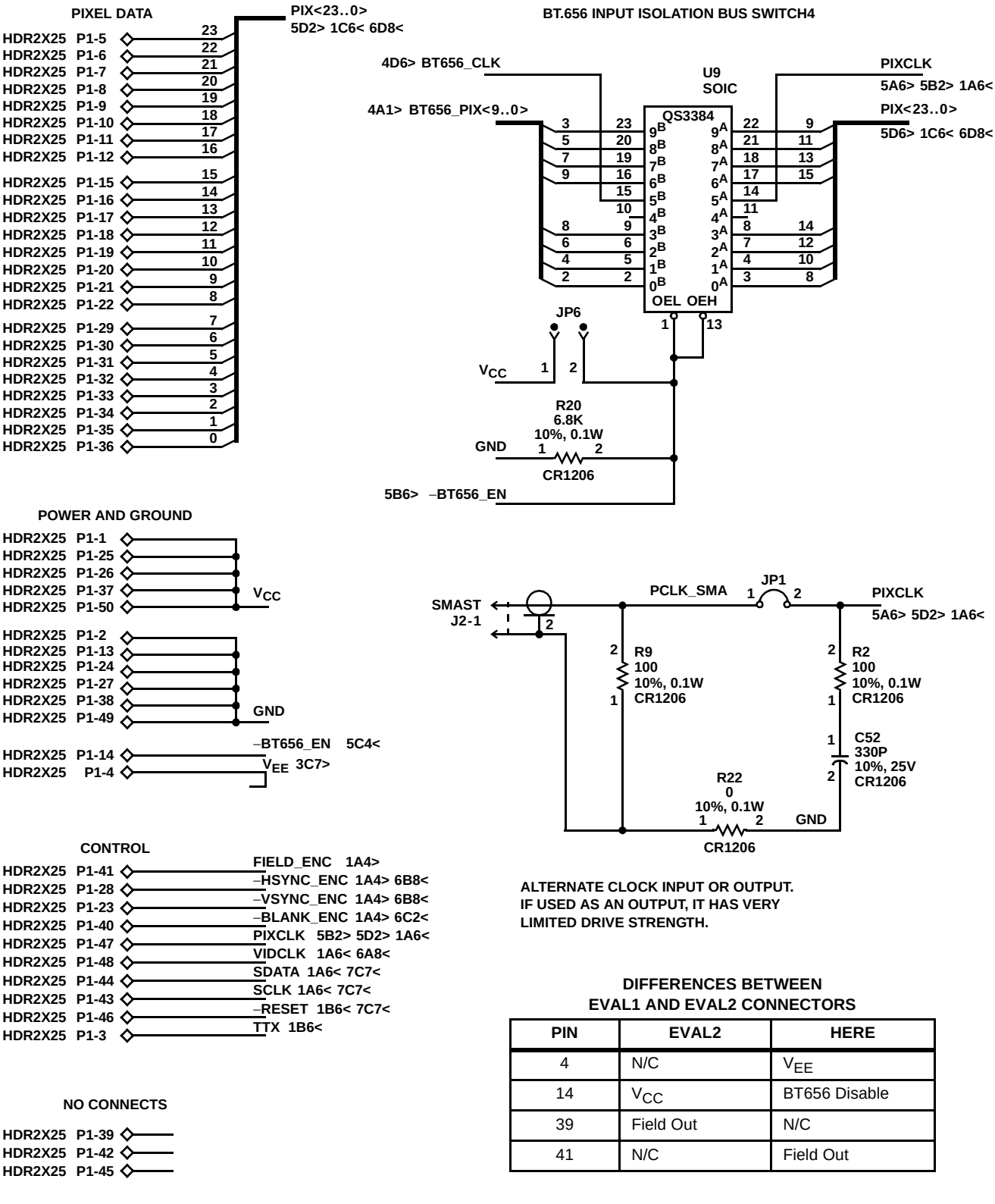


FIGURE 7. BT.656 INPUT

HMP8154EVAL1 Evaluation Board Schematic Diagrams (Continued)



DIFFERENCES BETWEEN EVAL1 AND EVAL2 CONNECTORS

PIN	EVAL2	HERE
4	N/C	V_{EE}
14	V_{CC}	BT656 Disable
39	Field Out	N/C
41	N/C	Field Out

FIGURE 8. EVM1 CONNECTOR AND CLOCKS

HMP8154EVAL1 Evaluation Board Schematic Diagrams (Continued)

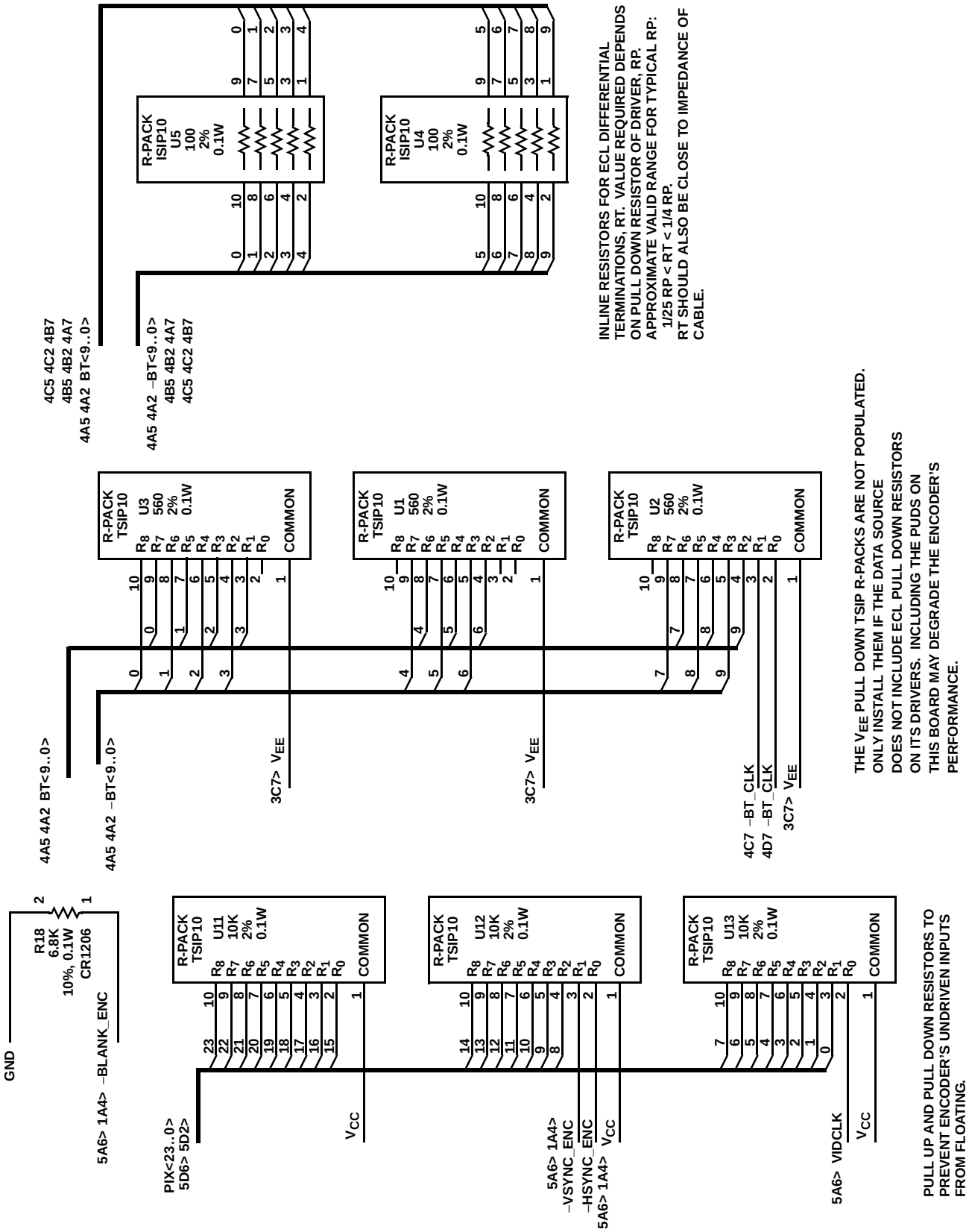


FIGURE 9. PUP/PUD TERMINATIONS

HMP8154EVAL1 Evaluation Board Schematic Diagrams (Continued)

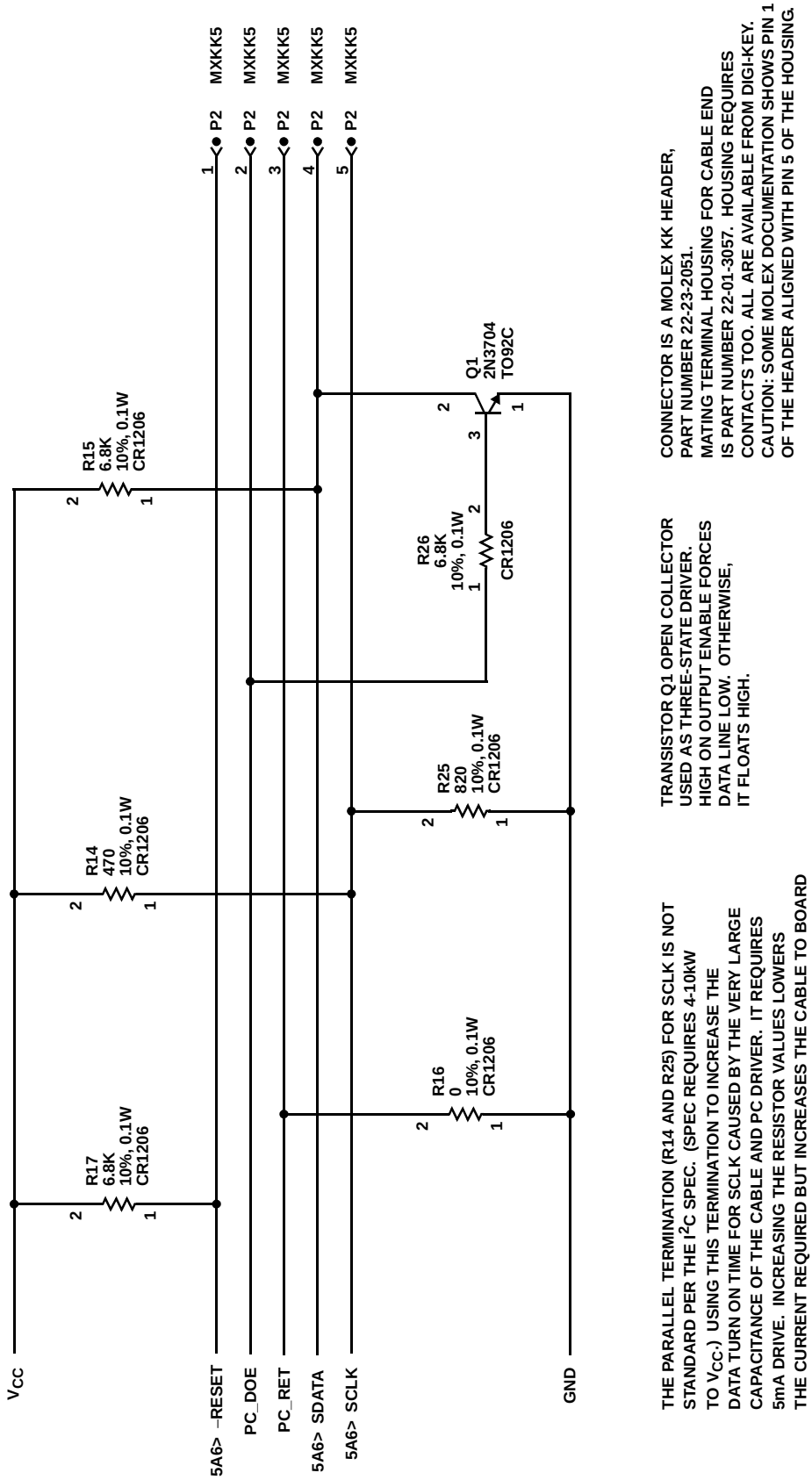


FIGURE 10. PC I^2C INTERFACE

HMP8154EVAL1 Evaluation Board Parts List

ITEM	QTY	REFERENCE DESIGNATOR	PART NAME	MANUFACTURER	PART NUMBER
1	8	C5, C21, C31, C34, C36, C46, C47, C50	CAPACITOR_CR1206-0.01µ, 25V, 10%	VARIOUS	?
2	17	C4, C22, C23, C32, C33, C35, C37-C39, C48, C49, C51, C53-C55, C58, C59	CAPACITOR_CR1206-0.1µ, 25V, 10%	VARIOUS	?
3	9	C9, C12, C16, C17, C25, C40, C41, C43, C52	CAPACITOR_CR1206-330P, 25V, 10%	VARIOUS	?
4	4	C10, C18, C27, C56	CAPACITOR_CR1206-39P, 25V, 10%	VARIOUS	?
5	4	C7, C14, C29, C44	CAPACITOR_CR1206-82P, 25V, 10%	VARIOUS	?
37	12	C6, C8, C11, C13, C15, C19, C26, C28, C30, C42, C45, C57	CAPACITOR_CR1206-DUMMY, 25V, 10%	NOT POPULATED	-
6	2	C2, C3	POLARCAP_THTANT-15µ, 15V, 10%	KEMET	T350E156K016AS
7	3	C1, C20, C24	POLARCAP_THTANT-4.7µ, 15V, 10%	KEMET	T350B475K016AS
8	1	D1	DIODE_TO92-ICL8069DCZR	INTERSIL	ICL8069DCZR
9	4	J3-J6	COAX_BNCST	AMPHENOL-RF	31-5329
10	1	J2	COAX_SMAST	JOHNSON COMPON.	142-0701-201
34	4	J7-J10	EPOINT_4H30	PLATED THRU-HOLE	IN PCB ARTWORK
12	1	J1	JCONNECTOR_DSUB25S	AMP	745967-7
13	1	J1	LOCKING_POST	AMP	206514-1
14	3	JP2, JP5, JP6	JUMPER2	BERG ELECTRONIC	69190-402
15	2	JP2, JP5	JUMPER_SHUNT	BERG ELECTRONIC	65474-010
16	3	JP1, JP3, JP4	ULOOP HEAVY GAUGE WIRE	BUS	
17	8	L2, L4, L5, L7-L9, L12, L13	INDUCTOR_CR1210-1.0µ, 30Q, 10%	DALE	IMC1210-1.0UH-10
18	4	L3, L6, L10, L11	INDUCTOR_CR1210-2.2µ, 30Q, 10%	DALE	IMC1210-2.2UH-10
19	1	L1	INDUCTOR_TH-FERRITE_BEAD,5A,TOL	DEXTER MAGNET ET AL	2743001111
20	1	P1	JCONNECTOR_HDR2X25	AMP	2-102973-5
38	1	P2	POST_MXKK5	MOLEX	22-23-2051
22	1	PCB	HMP815X_EVAL1	-	-
39	1	Q1	NPNBJT_TO92C-2N3704	NATIONAL SEMI	?
23	1	R5	POTENTIOM_TH-200, 0.5W, 10%	DALE	T93YA-200-10
24	8	R8, R10-R12, R16, R22-R24	RESISTOR_CR1206-0, 0.1W, 10%	VARIOUS	?
25	3	R1, R2, R9	RESISTOR_CR1206-100, 0.1W, 10%	VARIOUS	?
40	1	R14	RESISTOR_CR1206-470, 0.1W, 10%	VARIOUS	?
26	1	R4	RESISTOR_CR1206-51, 0.1W, 10%	VARIOUS	?

HMP8154EVAL1 Evaluation Board Parts List (Continued)

ITEM	QTY	REFERENCE DESIGNATOR	PART NAME	MANUFACTURER	PART NUMBER
28	7	R3, R15, R17, R18, R20, R21, R26	RESISTOR_CR1206-6.8K, 0.1W, 10%	VARIOUS	?
41	1	R25	RESISTOR_CR1206-820, 0.1W, 10%	VARIOUS	?
29	4	R6, R7, R13, R19	ESISTOR_CR1206-93.1, 0.1W, 1%	VARIOUS	?
30	3	U6-U8	10H125_PLCC	MOTOROLA	MC10H125FN
31	1	U10	HMP8154_MQFP	INTERSIL	HMP8156CN OR HMP8154CN
32	1	U9	QS3384_SOIC	QUALITY SEMI	QS3384SO
35	2	U4, U5	RESISTOR_ISIP10-100, 0.1W, 2%	VARIOUS	?
33	3	U11-U13	RESISTOR_TSIP10-10K, 0.1W, 2%	VARIOUS	?
36	3	U1-U3	RESISTOR_TSIP10-560, 0.1W, 2%	VARIOUS	?

HMP8154EVAL1 Evaluation Board Layout

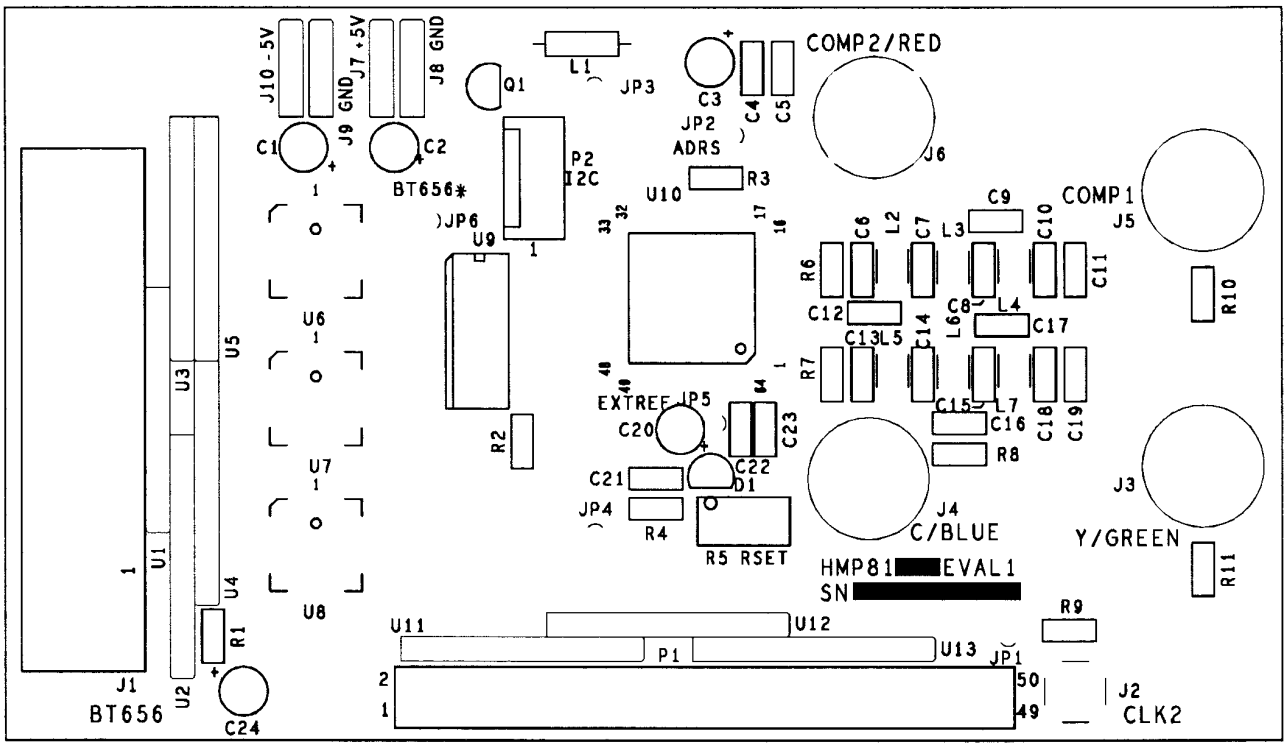


FIGURE 11. SILK SCREEN TOP

HMP8154EVAL1 Evaluation Board Layout (Continued)

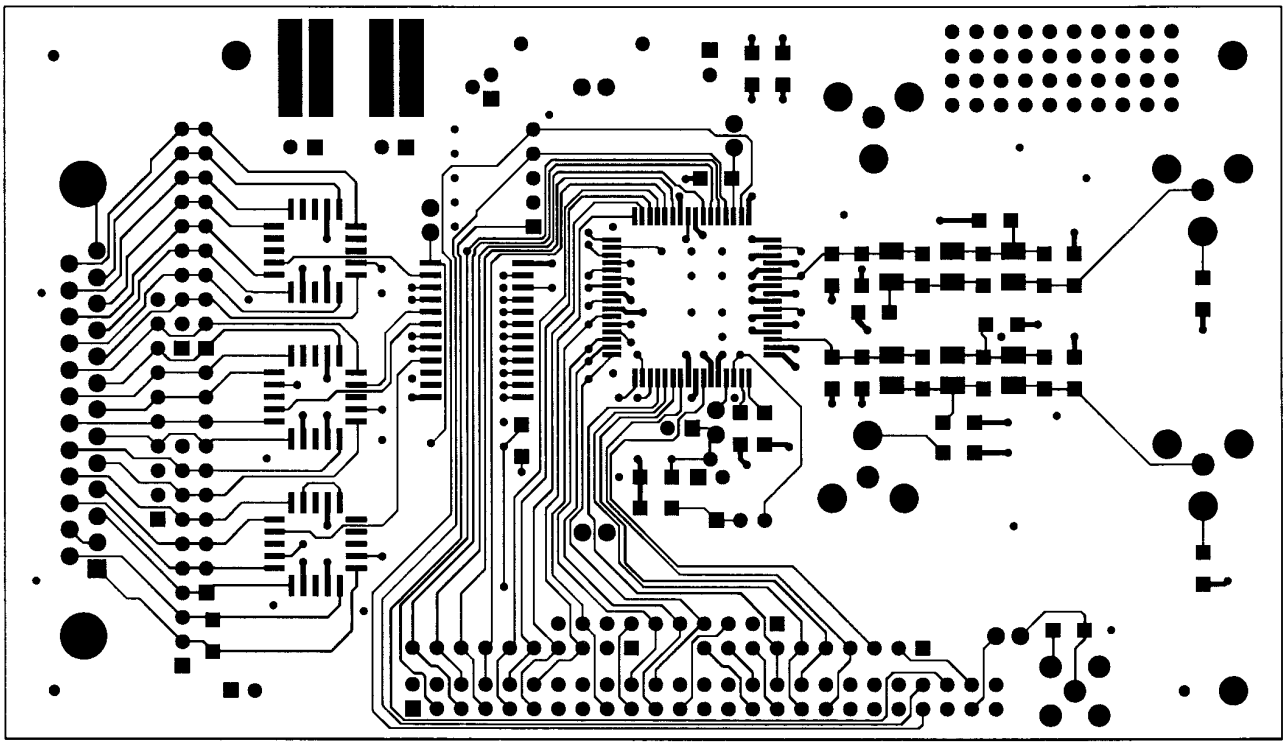


FIGURE 12. TOP LAYER COMPONENT SIDE

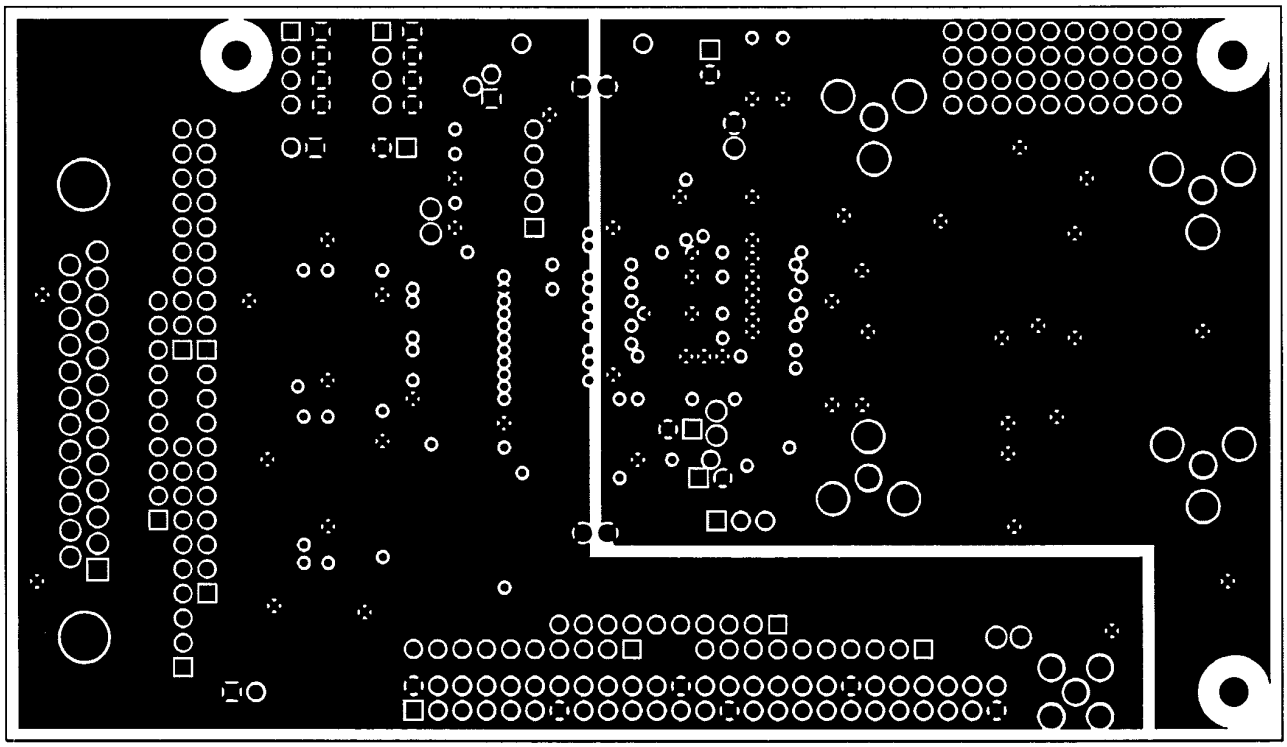


FIGURE 13. LAYER 2, GROUND

HMP8154EVAL1 Evaluation Board Layout (Continued)

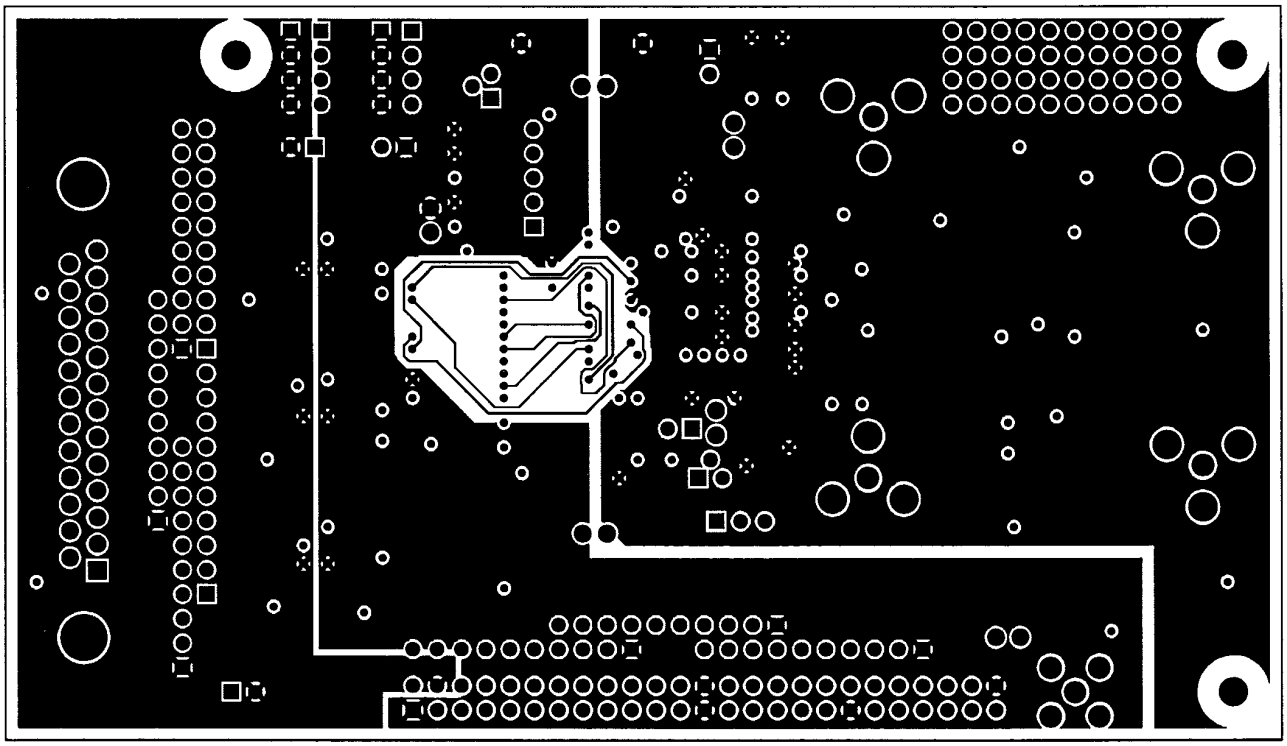


FIGURE 14. LAYER 3 V_{EE}, V_{CC}, V_{AA}

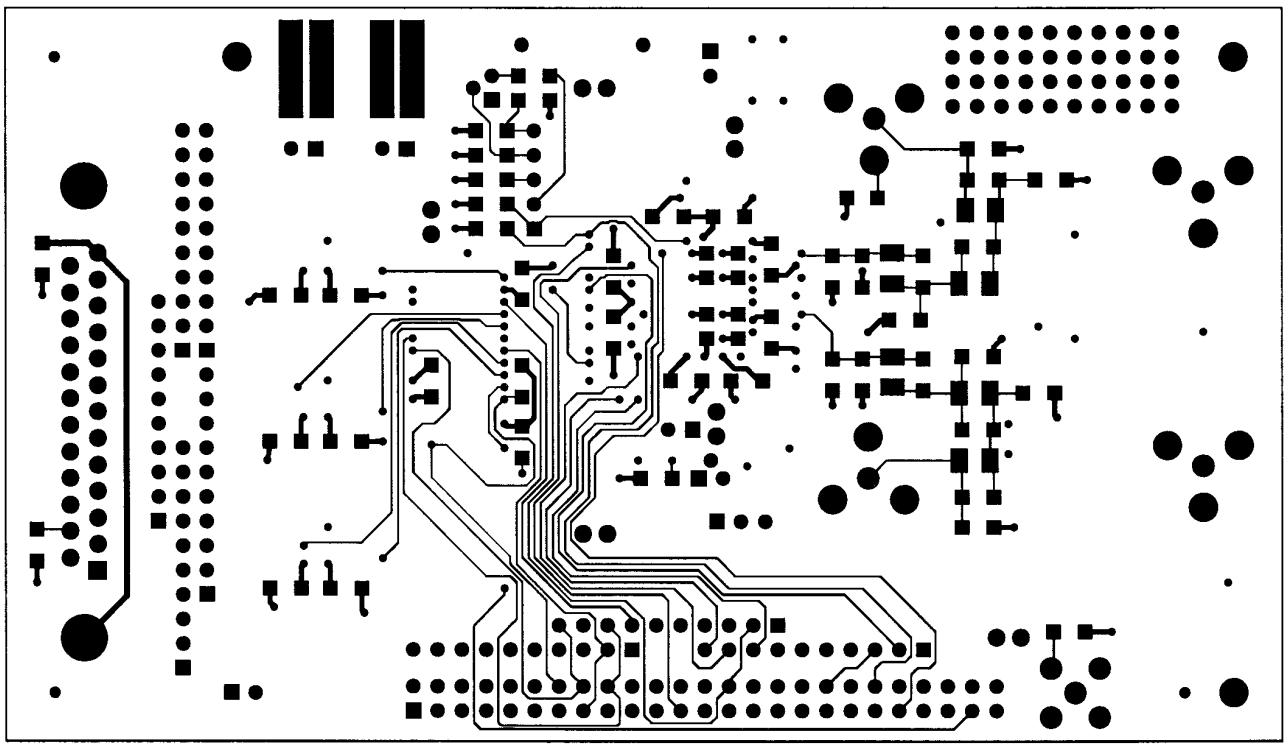


FIGURE 15. BOTTOM LAYER SOLDER SIDE

HMP8154EVAL1 Evaluation Board Layout (Continued)

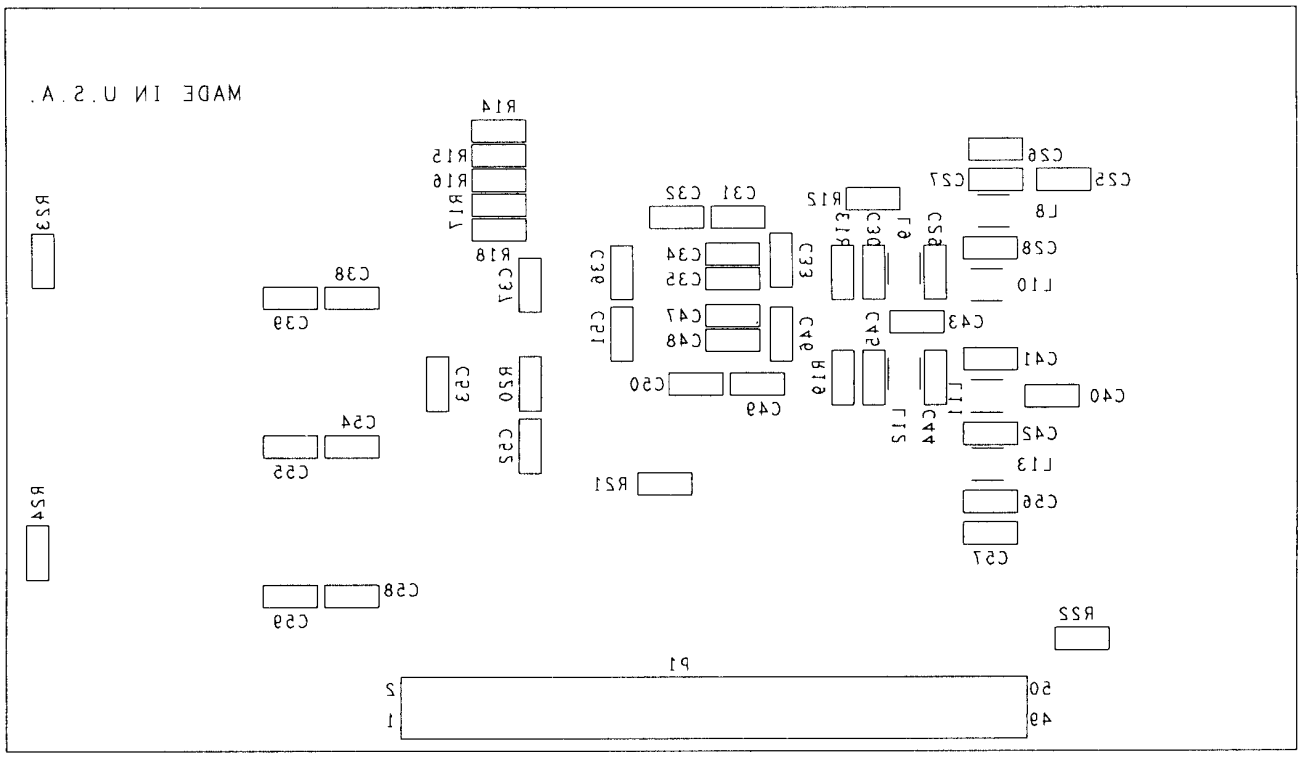


FIGURE 16. SILK SCREEN BOTTOM